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| 10/765,027 | 01/26/2004 | Kwan Ju Koh | 20059/PIA31191 | 1316 |

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| EXAMINER | |
|---|---|
| NOVACEK, CHRISTY L | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2822 | |

DATE MAILED: 04/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/765,027 | KOH, KWAN JU | |
| | Examiner | Art Unit | |
| | Christy L. Novacek | 2822 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *20 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-3 and 5-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 5-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

This office action is in response to the amendment and request for continued examination filed March 20, 2006.

### *Continued Examination Under 37 CFR 1.114*

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on March 20, 2006 has been entered.

### *Response to Amendment*

The limitations added to claim 1 are sufficient to overcome the Lee et al. (US 5,583,064) reference. Therefore, the rejections of claims 1-4, 6 and 7 as being unpatentable over Li et al. (US 6,309,933) in view of Yagashita et al. (US 6,607,952) and Lee et al. (US 5,583,064), and the claim 5 as being unpatentable over Li et al. and Yagashita et al. and Lee et al. and further in view of Bovaird (US 4,830,975) are hereby withdrawn.

### *Claim Objections*

Claim 12 is objected to for informalities. Claim 12 recites the limitation of "wherein forming the second oxide layer comprises oxidizing the exposed substrate". The limitation "the second oxide layer" lacks antecedent basis in the claims. Claim 8, upon which claim 12 depends, recites only one oxide layer – an oxide layer that is deposited on the polysilicon layer, not on the exposed substrate.

***Claim Rejections - 35 USC § 103***

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 1-3, 6, 7, 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Li et al. (US 6,309,933, previously cited) in view of Yagashita et al. (US 6,607,952, previously cited) and Wu (US 5,817,558).

Regarding claim 1, Li discloses forming a first oxide layer (12) on a surface of an active region of a substrate (10) and implanting ions thereinto for forming a lightly-doped drain (65) in the active region, forming a first nitride layer (22), removing a part of the first nitride layer and the first oxide layer and etching the substrate corresponding to the part by a depth of 800-1200 Angstroms to define a gate region, forming a second oxide layer (32) over an exposed portion of the substrate, implanting ions (38) into the substrate, removing the second oxide layer, depositing a gate insulating layer (40) and a polysilicon layer (42) into the removed parts of the first nitride layer and the first oxide layer, polishing until the first nitride layer is exposed, removing the nitride layer, depositing a conformal oxide layer (62) and a second nitride layer (64), etching the second nitride layer to form a gate sidewall (70) of nitride, implanting ions (72) into the substrate to form a source and drain (68) at both sides of the gate and removing an exposed oxide layer (col. 3, ln. 50 – col. 5, ln. 67).

Li does not disclose selectively forming a shallow trench isolation in a substrate. Yagashita discloses forming a shallow trench isolation (12/13) in the substrate of an integrated circuit in order to electrically isolate the active regions on the substrate so that multiple devices may be formed on the substrate, as is well-known in the art (col. 4, ln. 59-62). At the time of the

invention, it would have been obvious to one of ordinary skill in the art to form shallow trench isolation regions in the substrate of Li, as shown by Yagashita, because it is conventional in the art to form these regions for the purpose of electrically isolating active regions on an integrated circuit substrate.

Li discloses implanting the ions for forming the lightly-doped drain in the active region after the formation of the gate. Like Li, Wu discloses forming a MOSFET in a depression of a semiconductor substrate. Wu discloses that the ions for forming the lightly-doped drain and source implanted into the active region can be implanted before the gate depression region has been etched into the substrate (Fig. 2-5; col. 3, ln. 11-33). At the time of the invention, it would have been obvious to one of ordinary skill in the art to implant the ions that form the lightly-doped drain and source of Li either before or after the etching of the gate depression region because Wu teaches that implanting the ions before etching the depression results in a functional MOSFET product having low-doped source and drain positioned adjacent to each side of the gate and because when a prior art reference teaches a method which is the same as the method being claimed in an application under examination except for a difference in the order in which the steps of the method are conducted, the claimed method of the application is not patentable over the prior art method if no unexpected result occurs by the change in the order of the steps. See *Ex parte Rubin*, 128 USPQ 440 (Bd. App. 1959) (Prior art reference disclosing a process of making a laminated sheet wherein a base sheet is first coated with a metallic film and thereafter impregnated with a thermosetting material was held to render prima facie obvious claims directed to a process of making a laminated sheet by reversing the order of the prior art process steps.). See also *In re Burhans*, 154 F.2d 690, 69 USPQ 330 (CCPA 1946) (selection of any

order of performing process steps is prima facie obvious in the absence of new or unexpected results); *In re Gibson*, 39 F.2d 975, 5 USPQ 230 (CCPA 1930) (Selection of any order of mixing ingredients is prima facie obvious.).

Regarding claim 2, Li discloses that the substrate is a silicon substrate (col. 3, ln. 23-25).

Regarding claim 3, Yagashita discloses that the shallow trench isolation includes oxide layers (col. 4, ln. 59-62).

Regarding claim 6, Li discloses that the step of polishing until the nitride layer is exposed, includes a chemical mechanical polishing (CMP) step (col. 4, ln. 45-48).

Regarding claim 7, Li discloses that the second nitride layer is removed by an etch back process (col. 5, ln. 53-55).

Regarding claim 10, Li does not disclose selectively forming a shallow trench isolation in a substrate prior to implanting ions to form a LDD. Yagashita discloses forming a shallow trench isolation (12/13) in the substrate of an integrated circuit in order to electrically isolate the active regions on the substrate so that multiple devices may be formed on the substrate, as is well-known in the art (col. 4, ln. 59-62). Wu discloses that the isolation features can be formed prior to the implanting of LDD ions into the substrate. At the time of the invention, it would have been obvious to one of ordinary skill in the art to form shallow trench isolation regions in the substrate of Li, as shown by Yagashita, because it is conventional in the art to form these regions for the purpose of electrically isolating active regions on an integrated circuit substrate.

Regarding claim 11, Yagashita discloses that the shallow trench isolation can include an oxide layer (col. 4, ln. 59-62).

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Li et al. and Yagashita et al. and Wu as applied to claim 1 above, and further in view of Bovaird (US 4,830,975, previously cited).

Regarding claim 5, Li discloses growing the second oxide layer to have a thickness of about 100-150 Angstroms, but Li does not disclose the particular temperature range used to grow the oxide (col. 4, ln. 14-18). Like Li, Bovaird discloses oxidizing a silicon substrate to grow a thin layer of oxide thereon. Bovaird states that this thin oxide layer can be formed by a wet oxidation method at a temperature of 750°C (col. 2, ln. 64-65). At the time of the invention, it would have been obvious to one of ordinary skill in the art to grow the second oxide layer of Li by the oxidation process taught by Bovaird because Li does not disclose any particular temperature to be used and Bovaird teaches that a wet oxidation done at 750°C can successfully oxidize a thin layer of a silicon substrate.

Claims 8, 9 and 13-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Li et al. (US 6,309,933) in view of Wu (US 5,817,558).

Regarding claim 8, Li discloses forming a implanting ions into an active region of a substrate (10) to form a lightly-doped drain (65) (LDD) in the active region, forming a first nitride layer (22) in the active region, removing a part of the first nitride layer and etching the exposed substrate to a predetermined depth to define a gate region, implanting ions (38) into the substrate to control a voltage threshold of the device, forming a gate insulating layer (40) and a polysilicon layer (42) in the gate region, removing the first nitride layer, then depositing an oxide layer (62) and a second nitride layer (64) on the polysilicon layer, etching the second

nitride layer to form a gate sidewall (70), and implanting ions (72) into the substrate to form a source and drain (68) at sides of the gate (col. 3, ln. 50 – col. 5, ln. 67).

Li discloses implanting the ions for forming the lightly-doped drain in the active region after the formation of the gate. Like Li, Wu discloses forming a MOSFET in a depression of a semiconductor substrate. Wu discloses that the ions for forming the lightly-doped drain and source implanted into the active region can be implanted before the gate depression region has been etched into the substrate (Fig. 2-5; col. 3, ln. 11-33). At the time of the invention, it would have been obvious to one of ordinary skill in the art to implant the ions that form the lightly-doped drain and source of Li either before or after the etching of the gate depression region because Wu teaches that implanting the ions before etching the depression results in a functional MOSFET product having low-doped source and drain positioned adjacent to each side of the gate and because when a prior art reference teaches a method which is the same as the method being claimed in an application under examination except for a difference in the order in which the steps of the method are conducted, the claimed method of the application is not patentable over the prior art method if no unexpected result occurs by the change in the order of the steps. See *Ex parte Rubin*, 128 USPQ 440 (Bd. App. 1959) (Prior art reference disclosing a process of making a laminated sheet wherein a base sheet is first coated with a metallic film and thereafter impregnated with a thermosetting material was held to render prima facie obvious claims directed to a process of making a laminated sheet by reversing the order of the prior art process steps.). See also *In re Burhans*, 154 F.2d 690, 69 USPQ 330 (CCPA 1946) (selection of any order of performing process steps is prima facie obvious in the absence of new or unexpected

results); *In re Gibson*, 39 F.2d 975, 5 USPQ 230 (CCPA 1930) (Selection of any order of mixing ingredients is prima facie obvious.).

Regarding claim 9, Li discloses that the substrate is a silicon substrate (col. 3, ln. 23-25).

Regarding claim 13, Li discloses depositing the polysilicon onto the gate insulating layer in the gate region and chemical mechanical polishing the polysilicon (col. 4, ln. 38-45).

Regarding claim 14, Li discloses depositing the gate insulating layer in the gate region (col. 4, ln. 33-37).

Regarding claim 15, Li discloses that removing the second nitride layer involves etch back processing (col. 5, ln. 53-55).

Regarding claim 16, Li discloses that the predetermined depth is about 800-1200 Angstroms (col. 4, ln. 9-13).

Regarding claim 17, Li discloses, prior to implanting ions into the substrate to control the voltage threshold of the device, forming a second oxide layer (32) over an exposed portion of the substrate (col. 4, ln. 13-17).

Regarding claim 18, Li discloses, after implanting ions into the substrate to control the voltage threshold of the device, removing the second oxide layer (col. 4, ln. 30-33).

Regarding claim 19, Li discloses, after implanting ions into the substrate to form the source and drain, removing an exposed oxide layer (col. 5, ln. 62-67).

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Li et al. in view of Wu as applied to claim 8 above, and further in view of Bovaird (US 4,830,975).

Regarding claim 12, Li discloses growing a second oxide layer (32) on the exposed substrate such that it has a thickness of about 100-150 Angstroms, but Li does not disclose the

particular temperature range used to grow the oxide (col. 4, ln. 14-18). Like Li, Bovaird discloses oxidizing a silicon substrate to grow a thin layer of oxide thereon. Bovaird states that this thin oxide layer can be formed by a wet oxidation method at a temperature of 750°C (col. 2, ln. 64-65). At the time of the invention, it would have been obvious to one of ordinary skill in the art to grow the second oxide layer of Li by the oxidation process taught by Bovaird because Li does not disclose any particular temperature to be used and Bovaird teaches that a wet oxidation done at 750°C can successfully oxidize a thin layer of a silicon substrate.

### *Response to Arguments*

Applicant's arguments with respect to claims 1-3 and 5-19 have been considered but are moot in view of the new ground(s) of rejection.

### *Conclusion*

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Ni et al. (US 6,127,699) and Inumiya et al. (US 6,054,355) disclose implanting ions for forming a LDD region in a substrate and *then* etching the substrate to form a groove in which a gate of the device will be located (Fig. 2a-2H of Ni and Fig. 52A-56B of Inumiya).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christy L. Novacek whose telephone number is (571) 272-1839. The examiner can normally be reached on Monday-Thursday and alternate Fridays 7:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CLN
April 3, 2006

Michael Trinh
Primary Examiner